Serial No.: 10/044,344
Group Art Unit: 2826

AMENDMENTS TO THE SPECIFICATION

- Please amend the paragraph, which begins on page 3, line 7, as follows:

a'

Referring now to FIG. 2, therein is shown a cross-sectional view of FIG. 1 along line 2--2 looking up towards the wide top metal line 16 which is embedded in a dielectric layer 22. The via-sea 20 is shown more fully as vias 20a through 20i. The vias 20a through 20i are squares having a width "w" and spaced equal distances "W" apart. The distances that the vias are apart, such as the via 20a from the via 20d, would be such that "W" is slightly larger than <u>two</u> width<u>s</u> "w" and up to four times greater than width "w".

- Please amend the Abstract section which begins on page 8, line 1, as follows:

a2

ABSTRACT

A method is provided for an integrated circuit interconnect having a dielectric layer disposed between a wide top metal line and a wide bottom metal line. A via-sea in the dielectric layer connects the wide top and wide bottom metal lines by means of a first via having a width, a second via having a width and spaced more than ~~a~~ <u>two</u> width<u>s</u> away and less than four widths away from the first via. ~~The width and spacing of the vias reduce the occurrence of metal explosions which are known to reduce the power currying capability of the power lines and adversely affect the performance of the devices in the integrated circuit.~~